# Elevated substrate temperature implantation of 70 MeV Au in GaAs

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**Abstract**— One side polished, single crystal n+ GaAs of <100> orientation, have been implanted with 100 MeV 197Au to the dose of 1e14 ion/cm2 at room temperature and 70 MeV 197Au to the dose of 1e14 ion/cm2 at substrate temperature 100oC separately. Implanted samples were annealed at different temperatures from 100oC to 550oC. Ohmic contacts with Au-Ge-Ni alloy were made on sample before implantation. Temperature dependent current – voltage characteristics of samples implanted at room temperature & annealed at different temperature and room temperature current – voltage characteristics of samples implanted at elevated substrate temperature of 100oC & subsequently annealed at different temperature were recorded. Sample resistance of linear part of characteristics was considered for estimation of defects. The results were compared with similar study using 100 MeV Si and Sn.

We found that sample resistance and hence amount of defects after implantation defects depend on atomic mass of implanted ion and on substrate temperature during implantation. Annealing stages of defects also depends on atomic mass of implanted ion and during annealing cycle the defects are more stable for elevated substrate temperature implantation as compared to room temperature implantation.

**Index Terms**— Elevated temperature implantation, annealing, defects, GaAs.

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## 1 INTRODUCTION

Ion implantation is well known technique for the production of modern devices and integrated circuits in Si and compound semiconductor technologies. In case of III-V semiconductor, ion implantation has two important applications. The first one is to establish proper n- or p-type conductivity. The second is the implantation of suitable ions for electric isolation. This latter application is called implant isolation or isolation by ion irradiation [1]. Area of active research in MeV implantation includes studies on damage formation and disordering of GaAs super lattices. The damage resulting from the penetration of high energy ion irradiation can form amorphous layer below the surface which needs to be removed by an annealing process. As such, the annealing process of MeV implantation seems to be complicated than that of ion implantation at KeV energies [2]. It has been reported that in case of n+ GaAs, the implantation in the MeV range has diverse applications and also diverse areas of studied. Electrical characteristics show complex behavior with annealing treatment when n+ GaAs substrate is implanted in MeV range [3, 4]. Substrate temperature during implantation plays an important roll in damage production and there recovery. It is observed that the deeper defect levels are formed for samples implanted at elevated temperature [5]

In this paper we report the investigations of the room temperature implantation of 197Au in n+ GaAs to the dose of 1x1014 ions/cm2 and effect of the elevated substrate temperature (100oC) implantation of 197Au in n+ GaAs to the dose of 1x1014 ions/cm2 . We observe that there is reasonable change in the electrical characteristics of implanted n+ GaAs substrates after annealing both these samples at different temperatures from 100oC to 550oC. These investigations lead to better understanding in basic interaction processes between ion and semiconductor in the high-energy regime at different temperatures. Temperature dependent current – voltage measurements over the temperature range of -100oC to +100oC are reported for the sample implanted with 197Au to the dose of 1x1014 ions/cm2 at Room temperature. The results were compared with similar study with 28Si and 120Sn implantation in n+ GaAs.

## 2 EXPERIMENTAL DETAILS

In this experiment one side polished n+ GaAs substrate of size 7 mm X 7 mm and thickness 400 micron were used. The samples were carefully cleaned in organic solvents. Implantations were carried out on polished side at room temperature with 100 MeV 197Au ions and then separately at elevated substrate temperature of 100oC with 70 MeV 197Au ions to the dose of 1e14 ions/cm2 using the NEC 16 MV pelletron acclerator [6]. During implantation the beam current was held at 6-12 pnA and the Au beam was scanned to bombard the entire sample surface. The ohmic contacts were fabricated by vacuum deposition of uniform coating of Au-Ge-Ni alloy coating, both on the lower surface of each sample and dots with an area 0.0045 cm2, through a metal mask on the upper surface of each sample. The contacts made were then alloyed for 1 min in pure nitrogen ambient at 4500C. During the alloying process Au-Ge dissolves a thin region of GaAs substrate and later re-growth of Ge doped GaAs takes place which produces a heavily doped n++ region that provides the required ohmic contact. For these samples, the ohmic contacts were made before the implantation.

Samples were cut into small pieces of size about 3 mm

X 3 mm and different pieces were annealing over a range of temperatures from 100oC to 550oC. The annealing of samples was done isochronally for 10 min in high purity nitrogen ambient in a rapid thermal annealing system (RTA) system [7].

Current-Voltage (I-V) measurements between top and back contacts have been carried out for as-implanted samples and for the samples annealed at different temperature. The current-voltage (I-V) measurements were carried out at room temperature and over a range of sample temperatures from -100oC to +100oC using Keithley Electrometer 2400. I-V measurements were made on two to three dots on each sample and found to be repeatable. Although I-V measurements have been done on one selected dot on each sample after annealing treatment, in some cases they have been checked on more than one dot and found to be representative of the result. Sample resistance were recorded from linear part of the characteristic.

## 3 RESULTS AND DISCUSSIONS

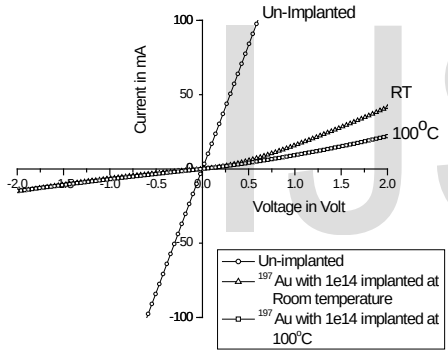


Figure 1. I -V Characteristics of un-implanted and as implanted samples.

Figure 1 shows the electrical characteristics of un-implanted substrate and as-implanted samples for dose 1X1014 ions/cm2 at room temperature and at elevated substrate temperature of 100oC. For implanted samples the I-V curves are weakly non-linear. We have estimated effective resistance in the linear portion of the curve where the series resistance is dominant. We have used the measured resistance values in this work instead of usual resistivity values because of uncertainty in the value of thickness to be used in calculating the resistivity from the measured resistance.

We observe that resistance of samples for room temperature implantation and elevated temperature implantation are 95Ω and 123Ω respectively. The low resistance indicates conduction via defect states. The density of the defect states must be reasonably high so that the electrons trapped in these levels can hop from one site to neighboring defect sites. Thus the electrical conduction in these samples is defect dominated [8, 9, 10]. Higher resistance of 123 Ω for elevated substrate temperature implantation indicates comparatively lower defect density.

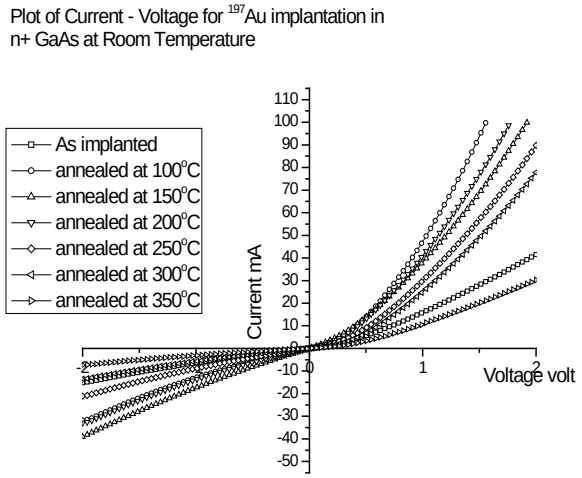


Figure 2. I -V Characteristics of as implanted and annealed samples implanted with 197 Au at room temperature.

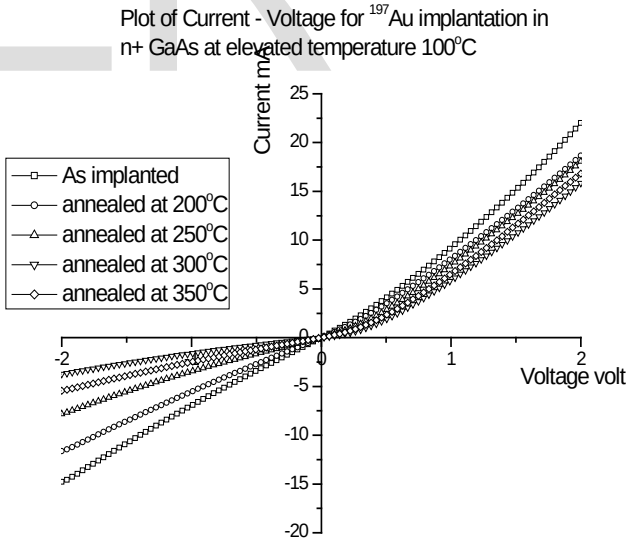


Figure 3. I -V Characteristics of as implanted and annealed samples implanted with 197 Au at elevated temperature 100oC.

Figure 2 shows the I-V characteristic of as implanted and annealed samples for room temperature implantation and figure 3 shows that of for elevated temperature (100oC) implantation. The as-implanted characteristics are fairly linear.

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The successive annealing treatment has made the curves more and more nonlinear. Table 1 shows room temperature sample resistance for both the implantation estimated from linear part of characteristics.

| Annealing Temp $^{o}$C | Resistance of $^{197}$Au implanted at Room Temp in Ω | Resistance of $^{197}$Au implanted at 100$^{o}$C in Ω |
|---|---|---|
| Room Temp. | 46.1 | -- |
| 100 | 14.8 | 135 |
| 150 | 18.8 | 160 |
| 200 | 17.1 | 165 |
| 250 | 21.4 | 241 |
| 300 | 24.6 | 477 |
| 350 | 62.5 | 324 |
| 450 | 37593 | 1401 |
| 550 | 373134 | 83134 |

Table 1:Resistance of samples annealed at different temperatures for 197Au implanted n+ GaAs at room temperature and at elevated temperature (100oC)

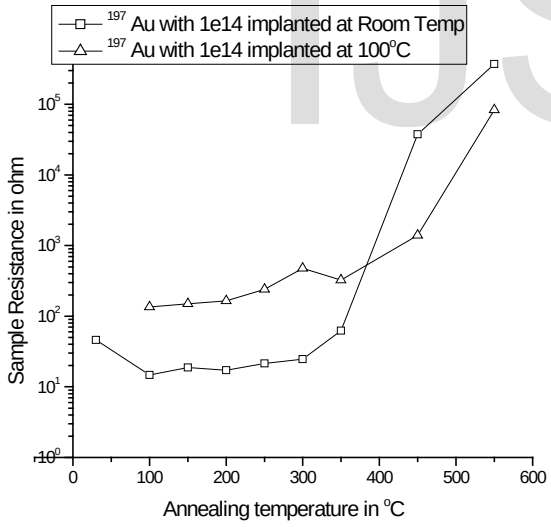


Figure 4. Effective resistance variation with annealing temperature.

Figure 4 shows room temperature values of effective resistance measured for different annealing temperatures for the sample implanted with the dose of 1X1014 ion/cm2 implanted at room temperature and at elevated temperature (100oC). We observe that there is not a much change in the substrate resistance for annealing up to 350oC for both implantations. This indicates that the conduction mechanism for the samples annealed up to 350oC may be hopping between the defect states. For elevated temperature implantation the samples resistances are slightly higher as compared to room temperature implantation. This may be due to low defect states compared to room temperature implantation.

After annealing to 4500 C resistivity of the sample implanted at room temperature increases suddenly. After this annealing stage at 450oC, the defects must have been annealed out and density of defect states in the band gap has been reduced so that hopping conduction no longer prevails, and therefore resistivity has suddenly increased. Higher values of resistance after annealing stage still in both the cases indicates that the carriers are trapped by the defect states still existing in the band gap and further annealing is required for the removal of defects [11].

In the similar experimental study by K V Sukhatankar et al [12] with 70 MeV 120Sn implantation in n+ GaAs at room temperature, the electrical properties of the irradiated samples were investigated after irradiation and annealing at various temperatures up to 1000 oC. It was found that electrical conduction is due to variable range hopping mechanism for sample annealed up to 450 oC. In these investigations, the defects were assumed to be created by nuclear energy loss.

Electrical characterization of a single crystal <100> orientation n-GaAs substrates implanted at room temperature with 100 MeV 28Si to a dose of 1x 1014 ions/ cm2 have been reported in literature [13]. The room temperature electrical characteristics of as implanted and samples annealed in the temperature range of 100-1000 oC have been studied. The current – voltage (I-V) curves show complex behavior with annealing temperature. For the samples annealed at and bellow 450 oC, the conductivity mechanism in the low temperature range was found to be dominated by variable range hopping. It has also been reported that in case of GaAs, the electrical characteristics shows complex behaviour with annealing treatment when it is implanted in MeV range.

The temperature dependence current-voltage (I-V) characteristics are helpful to understand conduction mechanisms taking place inside the sample. For the sample implanted with 100 MeV 197Au to the dose of 1e14 ions/cm2, the I-V characteristics have been studied over a temperature range of -100oC to +100oC.

Resistance of the samples implanted at room temperature and annealed up to 350oC satisfy the relation ρ(T)=ρ_0 e^((T_0/T)^(1⁄4) ) in the temperature range of -100oC to 0oC as shown in figure 5. That is in this temperature range the conduction is dominated by variable range hopping between defect energy levels in the forbidden gap.

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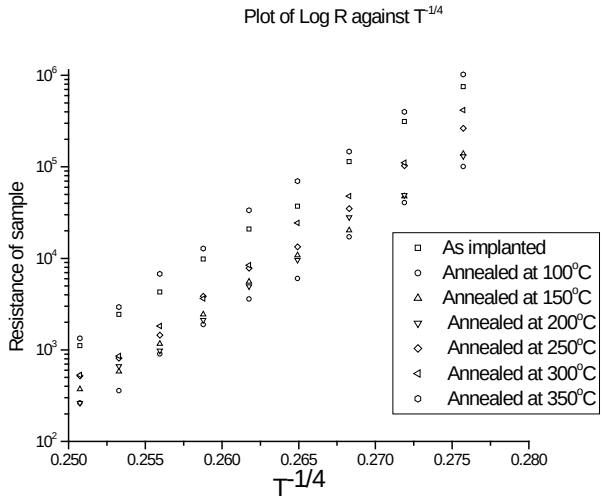


Figure 5. Log of sample resistance against T-1/4 for different annealing temperatures.

The values of T_0 obtained from the slopes of log R against T^(-1/4) are used to calculate localized state density at Fermi level N( Ef ) using N(E_F )=(c^4 α^3)/(T_0 k). The commonly obtained values of N(Ef) are found in the range of 1018 – 1019 cm-3eV-1. Similar observations were reported by A R Damale [14] with room temperature implantation of 28Si in n GaAs and by K V Sukhatankar in his Ph.D. thesis [15] (unpublished) with room temperature implantation of 120Sn in n+ GaAs. The values of N(Ef) corresponding to different ions are listed in table 2.

| Annealing Temp (°C) | $N(E_f)$ for $^{28}Si$ implanted n GaAs $x10^{18}$ ($cm^{-3}$ $eV^{-1}$) | $N(E_f)$ for $^{120}Sn$ implanted $n^+$ GaAs $x10^{18}$ ($cm^{-3}$ $eV^{-1}$) | $N(E_f)$ for $^{197}Au$ implanted $n^+$ GaAs $x10^{18}$ ($cm^{-3}$ $eV^{-1}$) |
|---|---|---|---|
| As implanted | 2932 | 1.78 | 1.870 |
| 100 | -- | 1.539 | 2.900 |
| 150 | 33.41 | -- | 2.595 |
| 200 | 26.83 | 1.446 | 2.554 |
| 250 | 22.30 | 1.424 | 2.167 |
| 300 | 21.89 | 1.033 | 2.012 |
| 350 | 17.10 | 0.918 | 1.766 |

Table 2:N(EF) at different annealing temperatures for 28Si, 120Sn and 197Au implanted samples implanted with the dose of 1e14 ions/cm2.

For each implantation, decreasing values of N(EF) with increasing annealing temperature, indicates that as the annealing temperature increases the defect concentration decreases which leads to small but finite increase in the resistance values. It has also been observed that defect density N(EF) varies with implanted ion. In case of comparatively lighter ion 28Si implantation defect densities are higher compared to those for 120Sn and 197Au implantation. The lighter ion implantation at MeV energy creates higher damages in the substrate.

## 4 CONCLUSION

We have implanted 100 Mev, 197Au ions in a single crystal n+ GaAs substrates at a fluence of 1X1014 ions/cm2 at room temperature and 70 Mev, 197Au ions in a single crystal n+ GaAs substrates at a fluence of 1X1014 ions/cm2 at 100oC. Samples were cut into smallpieces and annealed over temperature range of 100oC to 550oC. Electrical characteristics of the samples have been studied by current-voltage measurements and effective resistance was estimated. Current-voltage (I-V) characteristics are weekly nonlinear. Linear part of characteristics was considered for estimation of defects by calculating sample resistance. The results were compared with similar study using 100 MeV Si and Sn. It has been observed that the defects depend on implanted ion and substrate temperature during implantation. The defects are more stable for implantation for higher substrate temperature as compared to room temperature implantation.

## 5 ACKNOWLEDGEMENT

We are thankful to the scientific staff of Inter-University Accelerator Center, New Delhi for their kind cooperation during the implantation experiment. We also thank to Mr. Amit Shah, TIFR Mumbai and Prof. B M Arora, IIT Bombay for his guidance and help in the deposition of ohmic contacts.

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